Sergio BRUZZONE

ASIC DIGITAL DESIGNER & VERIFICATION ENGINEER

(25 years of experiences)

TECHNICAL SKILLS

ADVANCED
Cadence CAE tools (Analog Artist, Composer, Silicon Ensemble, Incisive, DFII)

Synopsys (Design Compiler)

Mentor CAE tools (Questasim);

FPGA tools (Xilinx, Altera)

Scripting languages UNIX Shell Scripting,Perl,TCL

SystemVerilog/OVM/UVM, Verilog, VHDL, ABV (SVA, PSL)

INTERMEDIATE
Mentor CAE tools - Formal verification (0-in)

Cadence – Formal verification (ifv, conformal)

SystemC, Specman/eRM, C, Verilog-AMS

PROFESSIONAL EXPERIENCE

From **January 2016** till **now NXP (Hamburg – Germany)**

Consultant for the AMS top level verification of a satellite/terrestrial radio (RF analog front end) using Verilog AMS and Verilog/VHDL for the RTL blocks.

From **November 2015** till **February 2016 Panthronics (Graz - Austria)**

Consultant for the AMS top level verification in an UVM environment to verify a standard product for NFC applications.

I developed all the UVC (UART, I2C, SPI, SWP, bus master, register map using XML/IPXACT), verified an in-house uC and created the top/block level simulation environment, including also some third party UVC

From **April 2015** till **July 2015 Freescale (Toulouse - France)**

Consultant for the AMS top level verification in an UVM environment to verify a standard product for the power management in the automotive/industrial sector

From **September 2014** till **March 2015 Huawei (Leuven - Belgium)**

Consultant for the design/verification of a multi standard RF transceiver (up to 10 GHz internal clock using differential clock logic). I created a random constrainted verification environment, based on Verilog/TCL and analog models

From **March 2014 till August 2014 ST Microelectronics (Sophia Antipolis - France)**

Consultant for a SOC with the BU IMG/DAP including many IPs (Cortex-M4, A53, Ceva DSP, GPU) (SOC level verification using mainly Mentor tools: Codelink + Questasim + SystemVerilog/UVM)

From **August 2011 till February 2014 NXP (Graz – Austria)**

Consultant for different projects related to Smart Cards & Security ICs (IC design & Verification using mainly Cadence tools, including also AMS verification)

From **December 2010 till July 2011 Infineon WLS (Linz – Austria)**

Consultant for a project in the wireless division of Infineon (now acquired by Intel) for the **digital design and verification** of a multistandard RF transceiver including an RF AFE, several microcontrollers, dedicated DSP structures, PMU, analog blocks.

From **January 2008 until January 2009 Infineon (Munich – Germany)**

Consultant in the Automotive Power division dealing with the **design** and **digital & AMS verification** of a **SOC** including a uC and several analog/power modules.

From **October 2004** to **December 2007 Olivetti (Ivrea - Italy)**

Consultant for an **ASICs/SOCs design** and **architectural design** of several products for printing&imaging (fax, xDSL, impact and ink-jet printers/MFP, WiFi print servers)

Involved in the design, AMS modeling and in the verification/validation of a new ink-jet print head (MEMS)

During **2004 AMS (Graz – Austria/Pisa - Italy)**

Consultant the **design, digital & AMS verification and PnR of ASICs** for automotive applications (door opening transceiver)

From **April 2002** to **December 2003 Atmel (Rome – Italy)**

Design Integration Manager. charged of the HW development (ASIC design, boards and emulation platforms).

Responsible for the design and manufacturing of a SOC including an ARM processor with several peripherals and a proprietary floating point DSP (1Gflops/1.5Gops at 100MHz) for radar, audio, super-computers applications.

AMS design, digital modeling & AMS verification of multi-port register files

From **March 2001** to **March 2002 Philips SC (Sophia Antipolis – France)**

Application Section Manager. in the Business Line Cellular Infrastructure of the Business Unit Mobile Communications.

Involved in the design of a HW platform for the development of SOC solutions including DSPs and Microprocessors. The BL-CI took advantage of my previous experiences in the telecom field to tune the strategical activities on 2.5G and 3G products.

From **January 2000** to **February 2001 Infineon (Graz – Austria)**

Technical Project Leader in the "Chip Card & Security Applications" Business Unit developing ASICs for Security Applications. I led the development of a SoC including a securized microcontroller and dedicated crypto-engines.

From **January 1998** to **December 1999 AMS (Graz - Austria)**

Design support engineer both for internal business units and the external customers, developing the new 0.35um CMOS library, and in the telecommunication business unit as **analog-digital designer**.

From **February 1990** to **December 1997 Marconi (Genova - Italy)**

ASIC designer and **ASIC design support** for telecom and military applications.

Functionally responsible for all the redesign activities and the technological decisions for the redesign and new developments of ASICs for the following applications: Sonet/SDH, PON, PDH, GSM.

From **October 1988** to **January 1990 Military Service (Roma-Nettuno - Italy)**

I served as **lieutenant in the Army** (Corpo Tecnico dell'Esercito).

From **June 1988** to **September 1988** Marconi (Genova – Italy)

Stage as **HW designer** in the Military Telecomunication BU.

EDUCATION

1982 – 1988 First class Degree in Electronic Engineering (cum laude) - University of Genoa

2009 Certified as **PMP** (Project Manager Professional) by PMI

LANGUAGES

French	: Fluent	**English**	: Fluent
German	: Fluent	**Italian**	: Mother tongue

OTHERS

Italian citizenship